

Balancing capacitively split DC link of three-level inverters

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Abstract: Nowadays, electric vehicles are playing an increasingly important role in transport. In everyday life, this is most evident in passenger cars, but at the same time, there are huge advances in freight transport and aviation. In order to maintain this developing trend, developers are striving to achieve the highest possible power density and maximum efficiency. With this increased efficiency comes longer driving range, thus electric car industry could take a bigger slice of the urban commuter traffic. Due to this trend, the use of multilevel, mainly three-level inverters has become widespread. The main advantage of a three-level inverter over the simpler two-level inverter is that it has a lower output current ripple, thus reducing switching losses and electronic noises. Capacitively split DC link topologies include NPC (Neutral Point Clamped) and T-type topologies.

Introduction

Since the batteries used in vehicles have a single output voltage level, it is necessary to use DC link capacitors to divide the voltage for the application of these inverters. Voltage imbalances of the DC link capacitors can even lead to damage semiconductors. An economical solution to this problem can be provided in software by using modulation techniques that balance the voltage of the capacitors. This paper describes voltage balancing techniques that can be applied to the above-mentioned topologies. The selection of the methods is based partly on literature and partly on new individual ideas. The problems encountered at the different operation points and their solutions are discussed. The viability of the solutions is verified by computer simulation.

There are different solutions to ensure the desired three-phase voltage at the outlets of a three-level inverter. One common alternative is the space vector approach, where a voltage vector is assigned to each switching state, and then a modulation algorithm generates the required rotating voltage space vector as a weighted sum of several space vectors. In the case of a three-level inverter, three voltage levels can be switched in three phases, so a total of $3^3 = 27$ switching states can be distinguished. Figure 1 illustrates the length and direction of the vectors corresponding to the 27 switching states. The total hexagon can be split into six triangles since it is sufficient to determine the weighting of the vectors of a PWM cycle for one triangle and then proceed in the same way for the others. [1]–[3]

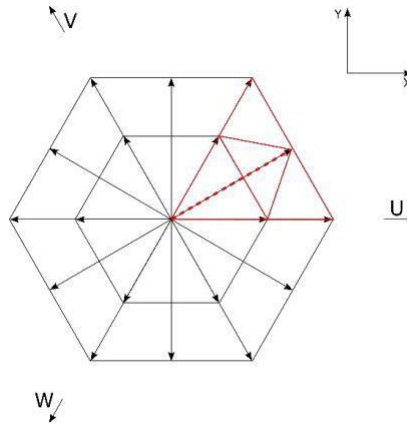


Figure 1
Space vectors of a three-level inverter

The short vectors can be reached with different switching states, for example $\left[\frac{+U_{DC}}{2}; 0; 0\right]$ and $\left[0; \frac{-U_{DC}}{2}; \frac{-U_{DC}}{2}\right]$ switches produce the same space vector. Since these vectors modify the midpoint voltage in different directions, it is possible to balance the voltage of the DC capacitors by appropriately weighting the two vectors within the PWM cycle. In the literature, different solutions are proposed for the splitting of the plane defined by space vectors. A triangle can be divided into four (Figure 1 red lines) [4] or six (Figure 1 dashed red line) [5] sectors. The two midpoint voltage-varying vectors are weighted according to the sector in which the resultant vector is situated.

The use of a carrier signal is another method of controlling a three-level inverter. In this case the output voltage levels, and thus the control signals of the semiconductors, can be determined by comparing the reference voltage signals with two triangular carrier signals (Figure 7). By shifting these reference signals up or down, the power from the positive and negative rails can be controlled and therefore the midpoint voltage also can be controlled. [6]

The paper presents the architectures, advantages, disadvantages and switching states of various three-level inverter topologies in chapter 2. Chapter 3 discusses the model-based implementation of the NPC topology, while chapter 4 describes the symmetrical modulation method of voltage balancing.

Topologies

NPC

The NPC (Neutral Point Clamped) topology consists of ten semiconductors per bridge: 4 switching elements (usually IGBTs), 4 diodes connected in parallel, and 2 clamping diodes. The input of the module is the voltage of a battery, which is split by the module capacitively in order to provide three voltage levels: positive, negative and the midpoint voltage $(+\frac{U_{DC}}{2}, N, -\frac{U_{DC}}{2})$. The output is the three-phase (U, V, W) sine voltage system. [7]

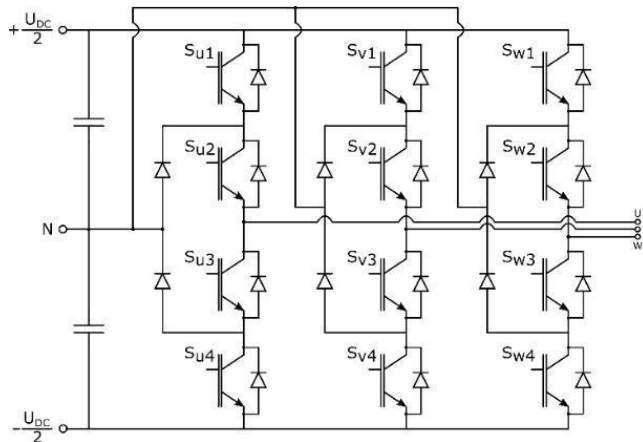


Figure 2
NPC inverter

In the NPC topology, all three voltage levels are switched to the output through two semiconductors, so diodes and IGBTs must handle only the half of the DC voltage, so switching loss and current ripple are both low.

T-type

In comparison with the NPC, the t-type contains only 8 semiconductors per bridge: 4 IGBTs and 4 diodes. Since the current flows through only one semiconductor when the half-voltages are switched, the conduction loss is lower than the NPC's. A disadvantage of the topology is that it cannot be built from simple two-level bridge modules because emitter pins of S2 and S3 are connected.

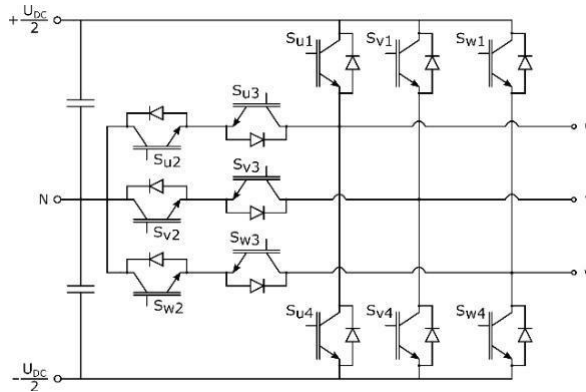


Figure 3
T-type inverter

In case of the T-type, S1 and S4 must be able to withstand the full DC voltage, as they are used to switch the $+\frac{U_{DC}}{2}$ or the $-\frac{U_{DC}}{2}$ voltage to the output. The midpoint voltage is switched to the output via S2 and S3, so they must handle only the half of the DC voltage. [7]

Simulation model of NPC

The purpose of the model is to study the behaviour of the midpoint voltage. Since the load is not relevant, only the output voltages are calculated, and the measured feedback current is replaced by a three-phase sine wave generator. Thus, the current, voltage and phase angle values can be specified in the MATLAB script.

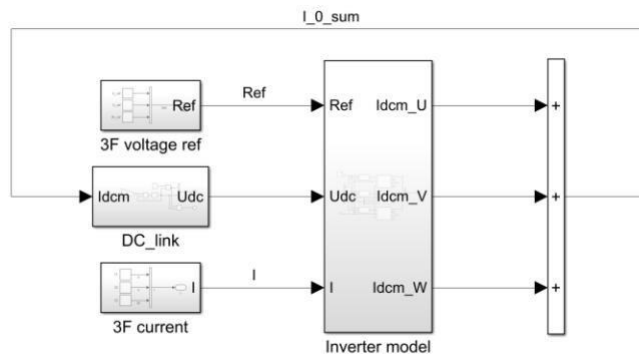


Figure 4
Model of the NPC inverter and its environment

DC link

The DC link is modelled from a simplified circuit with only one capacitor between the zero potential and the midpoint rail. In this case, the current of the midpoint rail is equal to the current of the capacitor, so Equation 1 can be used to calculate the voltage of the capacitor, which is equal to the midpoint voltage.

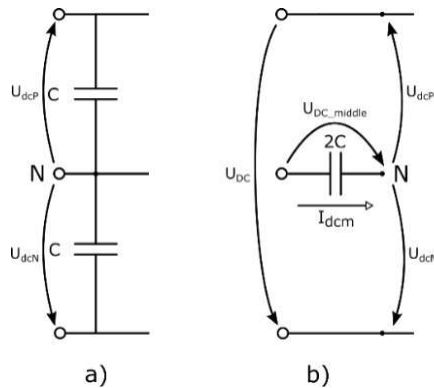


Figure 5
DC link model: a) Original, b) Simplified

$$U_c(t) = U_c(0) + \frac{1}{C} \cdot \int_0^t I_c(t') dt' \quad (1)$$

Inverter model

The input of the model is the DC voltages, the reference voltages, and the phase currents. Based on these signals, the block determines the inverter output voltages and the midpoint current. In the PWM_UVW block, the reference voltages are divided by either the positive or the negative DC rail voltage, depending on their sign, to produce the duty cycle. The duty cycle is then compared to the 10 kHz triangle carrier signals to produce PWM signals.

Based on the PWM signals, the control signals of the switching elements can be generated, so S1 and S2 are on for the positive half voltage, S3 and S4 for the negative half voltage, and S2 and S3 for the medium voltage. In order to make the model as realistic as possible, a switch-on dead time is applied. Since semiconductors have turn-on and turn-off delays, a bridge short-circuit can easily occur without dead time. Logical gates are used in the VoltageCalc blocks to determine the output voltages of the inverter. When the output voltage is equal to the midpoint voltage, the midpoint current is equal to the phase current, in all other cases it is zero. Following this logic, the sum of the mid-point currents in the three phases can be determined, so the DC link capacitor voltage can also be calculated.

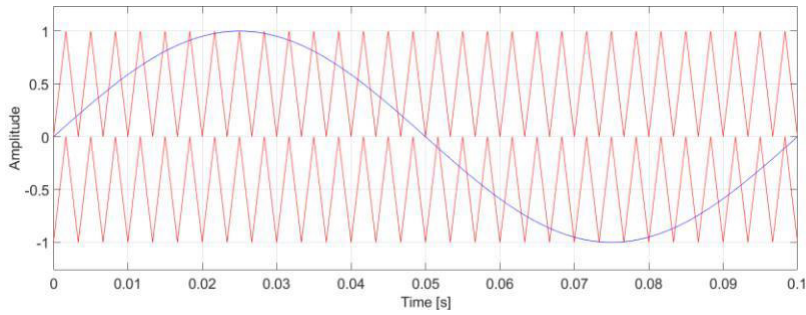


Figure 7
PWM generation

Midpoint voltage balance of the NPC

By running the model presented in the previous chapter, it can be seen that the inverter's midpoint voltage is unstable (Figure 8). The simulation was run based on the parameters in the table below.

Table 1
Operating point parameters

f_{sw}	10kHz	switching frequency
f	50Hz	Fundamental frequency
U_{dc}	800V	DC voltage
$\hat{U}_{ref}$	100V	peak value of the voltage ref.
$\hat{I}$	200A	peak value of the current ref.
φ	0	phase shift
C_{DClink}	10mF	DC link capacitor
t_{DT}	200ns	deadtime

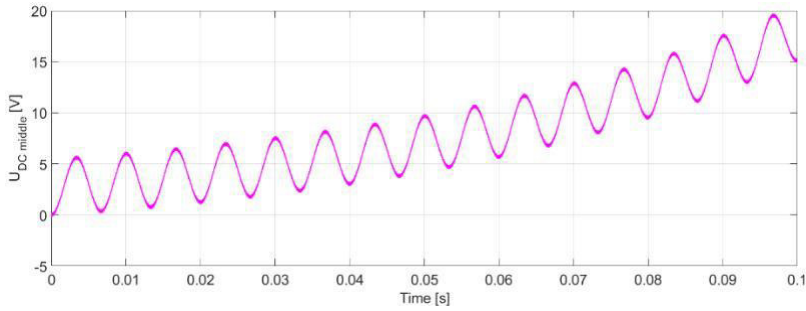


Figure 8
Midpoint voltage without balance

The reason of the instability is that the reference voltages are divided by the positive or the negative rail voltage when the duty cycles are generated, so at positive power flow (motor mode) a positive feedback is generated in the control loop.

Symmetrical modulation

The maximum line voltage of a three-phase inverter is equal to the DC voltage, and the maximum phase voltage is equal to $\frac{U_{DC}}{\sqrt{3}}$. However, with a simple sinusoidal modulation, only the half of the DC voltage can be reached as phase voltage, because the duty cycles are limited between 1 and -1. In order to use the maximum voltage that can be physically reached, different modulation techniques are used. One of these solutions is symmetrical modulation, where the difference between the most positive phase voltage and the positive rail voltage must be equal to the difference between the most negative voltage and the negative rail voltage. To achieve this, the reference voltage must be shifted by a U_0 voltage, which can be calculated from Formula 2, where U_{DCP} is the positive rail voltage, U_{dcN} is the negative rail voltage, U_{max} is the maximum phase voltage at that moment and U_{min} is the minimum phase voltage. Rearranging the formula gives Formula 3.

$$U_{dcP} - (U_{max} + U_0) = (U_{min} + U_0) - U_{dcN} \quad (2)$$

$$U_0 = \frac{1}{2} \cdot (U_{DCP} + U_{dcN} - U_{max} - U_{min}) \quad (3)$$

Motor mode

The direction of the energy at the working point described above is positive, which is motor mode for an electric machine. By applying symmetrical modulation to this operating point, the obtained voltage reference and midpoint voltage charts are shown in Figure 9. It can be noticed that the DC midpoint voltage ripple is reduced, and the system stabilizes. This is explained by the fact that when symmetrical modulation is applied, the duty cycles are shifted to the middle of the available voltage range.

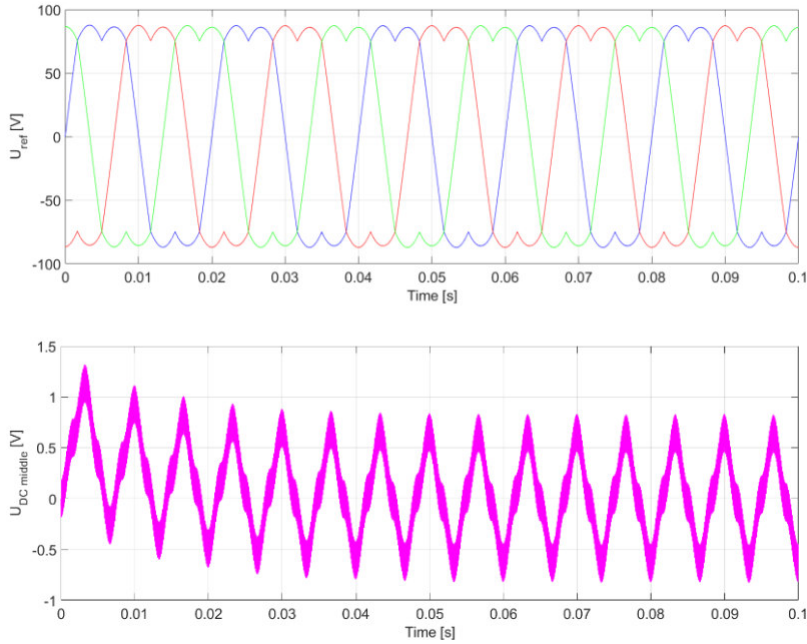


Figure 9

Voltage references and the midpoint voltage, using symmetrical modulation

Generator mode

Based on the previous chapter, it is predictable that in generator mode, the use of symmetrical modulation increases the instability. By changing the phase shift to $\frac{(2\cdot\pi)}{3}$, the direction of the power is reversed. Running the simulation in this way gives the midpoint voltage shown in Figure 10. It is clearly visible that symmetrical modulation is not sufficient to achieve stability, therefore a proportional controller is also required in the model. Thus, the reference voltages are shifted also by an error signal multiplied by a proportional factor, where the error signal is the deviation of the midpoint voltage from zero. The sign of the proportional factor is negative in generator mode. [8]

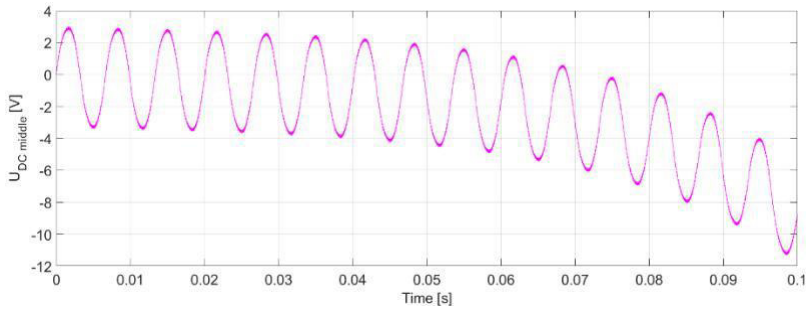


Figure 10

Midpoint voltage in generator mode, using symmetrical modulation

Which proportional factor is required to eliminate instability in generator mode? The principle of the investigation is to calculate the average value of the midpoint voltage for an ε imbalance error. For this error, regulating the average value to zero gives exactly the limit of stability, so using a controller with a higher value than the calculated will stabilize the system.

Since the midpoint voltage oscillates with three times of the fundamental frequency, it is sufficient to make the calculation for one third of the period time. To do this, the midpoint current must be integrated in several steps. I have chosen the $\left[\frac{1}{6}\pi; \frac{5}{6}\pi\right]$ section where the first phase voltage is the most positive (Figure 11)

First the time functions of the voltages must be determined to define the time function of the midpoint current. The obtained time functions are divided by the voltage of the positive or negative rail, depending on the sign, to calculate the time functions of the duty cycles. To ensure that the signs are correctly considered, the calculation was done in 8 steps. (Figure 11)

Using the time functions of the phase currents, the midpoint current can be determined from Formula 4, where $d(t)$ is the time function of the duty cycle and $I(t)$ is the time function of the phase current.

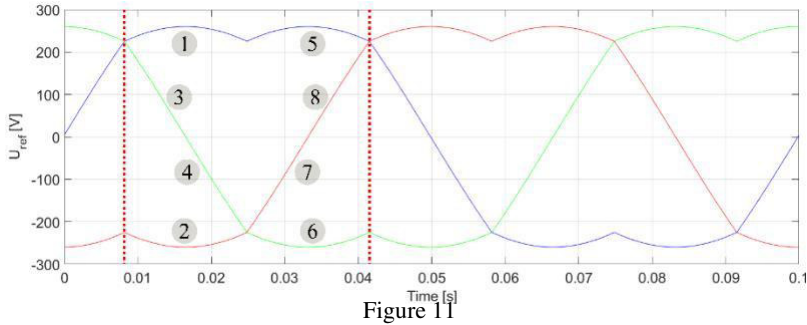
$$I_0(t) = (1 - d(t)) \cdot I(t) \quad (4)$$

The time function of the voltage of the 1 marked section in the figure is expressed by the Formula 5 and the time function of the phase current is given by the Formula 6, where I_{amp} is the current amplitude and φ is the phase shift of the current. By expressing the duty cycle and then rearranging the equations according to Formula 4, the time function of the midpoint current is obtained (Formula 7). In a similar way, the time function of the midpoint current can be determined for the other sections.

$$U_{amp} \cdot \sin(w \cdot t) + \frac{U_{amp}}{2} \left(\sin(w \cdot t) + \sin\left(w \cdot t - \frac{2}{3}\pi\right) \right) + (U_{dcP} + U_{dcN}) \cdot \left(\frac{1}{2} + P\right) \quad (5)$$

$$I_{amp} \cdot \sin(w \cdot t + \varphi) \quad (6)$$

$$\left(1 - \left(\frac{U_{amp}}{2 \cdot U_{dcP}} \cdot \left(\sin(w \cdot t) - \sin\left(w \cdot t - \frac{2}{3}\pi\right) \right) + \frac{U_{dcP} + U_{dcN}}{2 \cdot U_{dcP}} + \frac{P \cdot (U_{dcP} + U_{dcN})}{U_{dcP}} \right) \right) \cdot I_{amp} \cdot \sin(w \cdot t + \varphi) \quad (7)$$



The investigated one-third period

To determine the limits of the integrations, the zero-crossing location of the sign changing sections should be calculated. Then the sum of the integrals can be expressed symbolically by using the MATLAB Symbolic toolbox. By equalizing this sum to 0, the P proportional factor can be determined which, in absolute value, will produce the smallest change in the midpoint voltage. With the parameters described above, the proportional factor $P = -0.4061$ is the appropriate choice. The negative sign is caused by the generator mode, in motor mode a positive result is obtained.

The calculation above gives the proportional factor for the stability limit state. The upper chart of the Figure 12 clearly shows that with the calculated factor, the midpoint voltage stabilizes, but the average value is not zero. However, when the proportional factor is larger in absolute value than the calculated one. ($P = -1$), the average value of the midpoint voltage clearly approaches zero.

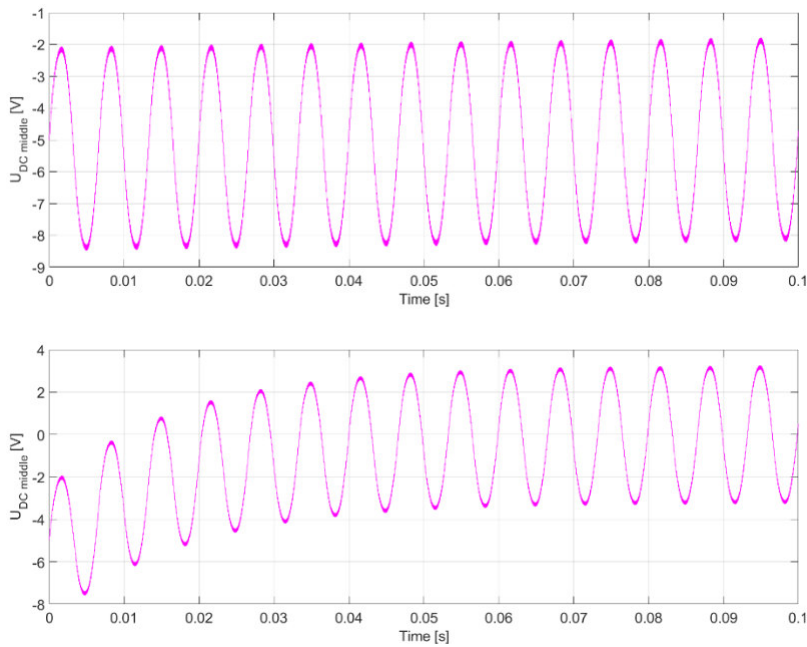


Figure 12

Midpoint voltage in generator mode with the calculated proportional factor (top),
 with factor higher in absolute value than the calculated one (bottom)

Conclusion

Based on the results of this paper, it can be concluded that symmetric modulation is sufficient to stabilize the midpoint voltage in motor mode. However, in generator mode, the use of a proportional controller is also necessary. These solutions can only be used if the sign of the power can be determined. Balancing in reactive operating points and further reduction of the ripple of the midpoint voltage are further improvement tasks.

References

- [1] S. Halasz and I. Varjasi, "Voltage Spectra of Three-Level Inverters with Three-Phase Modulation," 2006. doi: 10.1109/IPEMC.2006.4778072.
- [2] S. Halasz and I. Varjasi, "Small vector PWM strategies of three-level inverters," 2004. doi: 10.1109/ISIE.2004.1571996.
- [3] S. Halasz and I. Varjasi, "Analysis of three phase PWM strategies of three-level inverters." doi: 10.1109/SPEEDAM.2006.1649978.
- [4] Mr. S. Dasam and Dr. B. Sankerram, "Modeling of Dc Link Capacitor Voltage Balance in 3-Level Inverter Using Space Vector Modulation Technique," *Global Journal of researches in engineering Electrical and electronics engineering*, vol. 12, no. 5, 2012.
- [5] Y. Lai, Y.-K. Chou, and S.-Y. Pai, "Simple PWM Technique of Capacitor Voltage Balance for Three-Level Inverter with DC-link Voltage Sensor Only," 2007. doi: 10.1109/IECON.2007.4460351.
- [6] M. Swamy, K. Anuradha, and B. G. Babu, "DC level stabilization in Neutral Point Clamped multilevel inverters," Dec. 2015. doi: 10.1109/PCCCTSG.2015.7503907.
- [7] S. Ingo, "Semikron Application Note AN-1101." Oct. 12, 2015.
- [8] H. Kitidet and Y. Kumsuwan, "A CB-SVPWM control strategy for neutral-poin voltage balancing in three-level NPC inverters," Nov. 2017. doi: 10.1109/TENCON.2017.8228144.