Functional testing of PLC programs using FPGA-based Hardware-in-the-Loop simulation

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Abstract: Programmable logic controllers are essential tools in industrial automation, but functional testing of control programs is often difficult if the controlled equipment is not available or cannot be shut down. The aim of the research is to create an FPGA-based Hardware-in-the-Loop (HIL) environment that allows real-time testing of PLC programs without the physical manufacturing equipment. The case study is based on a pump performance testing station model, which was developed in a MATLAB/Simulink environment and then emulates the physical behaviour of the equipment by running on an FPGA in the form of HDL code. The control logic runs on a Siemens S7-1200 PLC, while the Digilent Nexys A7 FPGA simulates the signals of the system's sensors and actuators. In the current development phase, the HIL system model and system architecture have been completed, and PLC communication integration and FPGA implementation are in progress. The presentation will introduce the system architecture, the steps of model creation and HDL generation, as well as the experiences gained during implementation. At the current stage of research, the goal of development is to create a flexible HIL platform capable of examining real-time communication between the PLC and the simulated process, thereby enabling early fault detection and functional testing of the control logic. The system's expandability means that it can later be adapted to test various industrial processes, such as pump and valve control systems. The expected result of the project is a HIL test platform capable of safely and reproducibly modelling the behaviour of real industrial environments. Based on the results of the research so far, the FPGA-based HIL approach used in industry can be promisingly adapted for realistic and reproducible testing of PLC control programs.

Keywords: PLC; FPGA; HIL; Testing; Matlab; Simulink; Simulation

1 Introduction

Ensuring the reliability of PLC-based industrial control systems is essential, as faults can lead to downtime, financial loss, or safety hazards. However, functional

testing before commissioning is often limited because the controlled equipment may be unavailable, under assembly, or operating in a production line that cannot be stopped. As a result, developers frequently rely solely on documentation, which may differ from real system behaviour, making early error detection difficult.

To address these challenges, this work applies a Hardware-in-the-Loop (HIL) approach, enabling safe testing without physical equipment and allowing extreme or infrequent operating conditions to be examined. An FPGA is used to execute the plant model in real time, while the PLC runs the original control logic of a pump performance test station. The FPGA emulates the test bench's sensors and actuators through hardware-generated signals. The goal is to create a flexible HIL environment capable of reliably reproducing key process dynamics and supporting early-stage validation of industrial PLC programs.

2 Background & Problem Definition

Before commissioning, PLC programs often cannot be tested on real equipment due to limited availability or ongoing production, even though mistakes at this stage can cause significant losses. Documentation-based testing does not always reflect real operation, and errors—especially human ones—may remain undetected until later phases.

HIL systems offer a practical solution by allowing PLC programs to interact with a simulated plant model under realistic conditions. In this project, the controlled system is a pump performance test station that evaluates pumps based on their Q-H characteristic curve. Variations in flow or differential pressure can reveal manufacturing defects, making reliable testing essential.[3] [11]

Only the functions relevant to the Q-H determination such as flow measurement, differential-pressure calculation, and valve positioning were included in the model. In the proposed HIL setup, the PLC executes the original control logic while the FPGA emulates the hydraulic process and sensor behaviour. This approach provides a safe and reproducible environment for validating the control program and supports the development of more robust test procedures. [5] [6] [9]

3 System Architecture

The system is designed so that the control unit (PLC) and the simulated process (FPGA) communicate with each other in real time via direct electrical signals. In the HIL environment, the PLC plays the role of a controller of a real test bench, while the FPGA emulates the behaviour of the physical equipment. The modular

design of the system allows individual units to be easily expanded or modified during the development and testing process. [7]

The entire layout consists of three main subsystems:

1. **Control subsystem (PLC):** control of the technological process, running control logic, implementation of control algorithms.

2. **Simulation Subsystem (FPGA):** running the plant model in real time, generating sensor signals and actuator feedback.

3. **Communication and level shifting subsystem:** matching voltage level between two devices, galvanic isolation, and conversion of analogue and digital signals.

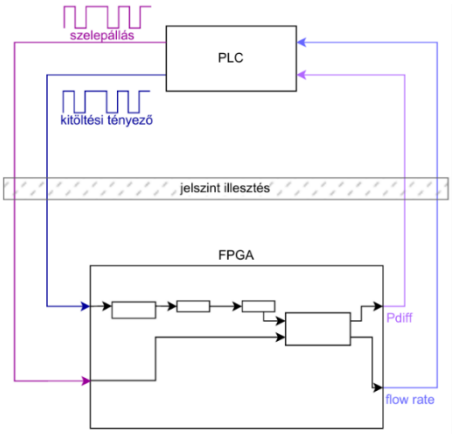

Figure 1 Connection of the subsystems [10]

The connection between the PLC and the FPGA is realized exclusively through physical input and output signals, without the use of a communication protocol. This ensures that the PLC program sees the same signal structures as in a real sensor and actuator network. This allows the results of the HIL test to be applied directly during the commissioning of the real system without any changes to the program.

Proper signal voltage level shifting is key in the system, as the FPGA uses 3.3V logic levels, while the PLC uses 24V industrial-grade input signals. The security of communication is ensured by galvanic isolation, which is realized by a uniquely designed optocoupler and transistor level shifting module.

The entire physical implementation is planned to carry out in a modular DIN rail arrangement, where the PLC, FPGA and level shifter modules are in separate units. This design is also suitable for laboratory demonstrations, educational environments, and industrial testing applications.

The synchronization of the system is due to the timing of the signals and the running speed of the HIL model. Although full cycle level synchronicity cannot be achieved (due to the different architecture of the PLC and FPGA), the system exhibits sufficiently deterministic behaviour to the extent required for functional tests.

4 Modelling and Implementation Approach

The first major milestone in the implementation of the system was the modelling of the pump testing water circuit and the related physical processes in a MATLAB/Simulink environment. The aim is to create a plant model that realistically reflects the dynamics of the hydraulic measuring circuit and is suitable for simulated recording of operating points controlled by the PLC. The structure of the model reflects the functional elements of the real equipment: motor control, hydraulic behaviour of the pump, pipeline elements, throttle valve dynamics, and volume flow and pressure measurement.

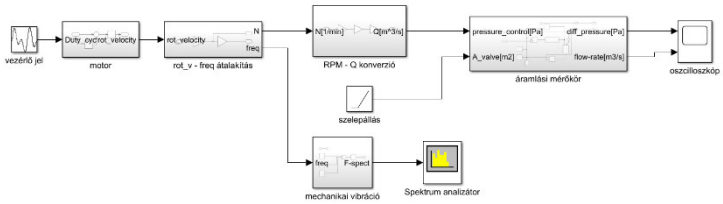

Figure 2 Simulation model assembled from functional sub-systems [10]

4.1 MATLAB/Simulink Model Structure

The model consists of several separate subsystems, which are functionally independent of each other and can be well adapted for future HIL implementation:

1. **Motor and drive model:** Receives the control signal and generates an equivalent speed. Detailed modelling of the electrical parameters was not necessary, as the RPM is the relevant information from the point of view of the PLC.

2. **Water transport circuit (pipe section + pump):** Models the characteristics of the pump and the resistance of the pipeline. Differential pressure is the basis for determining the working point.

3. **Flow Measurement Block:** Determines the volume flowing through the system. The model assumes an ideal measure, since the goal is to investigate regulatory behavior.

4. **Valve model (throttling):** Adjusts the hydraulic resistance of the circuit and thus the flow rate based on the valve position set by the servo motor.

The "inputs" of the model correspond to the future FPGA inputs: the fill factor of the motor control and the opening angle of the valve. And the "outputs" are the physical quantities required for the PLC: head (calculated from the differential pressure) and flow rate.

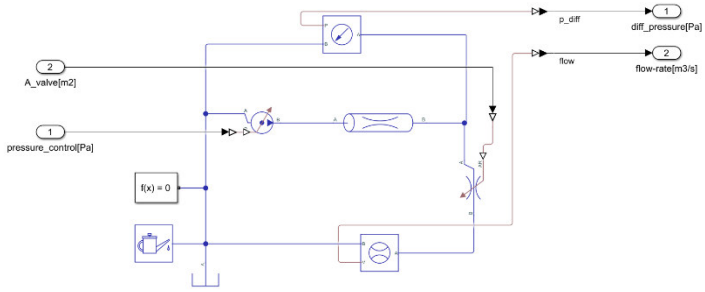

Figure 3 Sub-system of the measuring piping system [10]

During simulation-based validation the correct operation of the Simulink model was validated by recording a Q–H curve. With the gradual reduction of the volume flow (closing the valve), the differential pressure increased as expected, so that the model reproduced the characteristic curve characteristics of real pumps. The curve obtained because of the simulation is well approximated to the shape of typical factory Q–H curves.

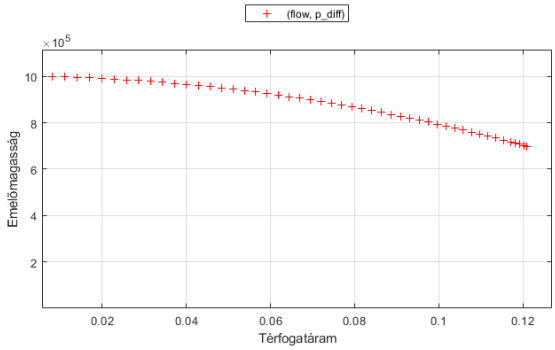

Figure 4 Pump performance curve as result of the simulation [10]

4.2 FPGA Implementation (High-Level Overview)

Based on the completed Simulink model, the functional units that need to be implemented on FPGAs have been determined. In the HIL system, the FPGA is responsible for the real-time reproduction of the simulated physical process and the generation of the sensor signals used by the PLC. About the VHDL implementation in this article we will only give you the overview you need to understand how it works:

1. The main components of the model are implemented as separate VHDL modules (motor, water circuit, valve).

2. Signal processing and data flow between subsystems follow the structure of the Simulink model.

3. The physical quantities (Q and H) are generated as quasi-analog signals for the PLC from PWM and RC filter.

4. The operation is deterministic, thanks to the high clock frequency of the FPGA, it is more accurate in time than a software-based simulation.

The VHDL architecture is not covered in detail in this article, but it is important to note that the modular design of the model allowed for the smooth implementation of the Simulink → HDL transition.

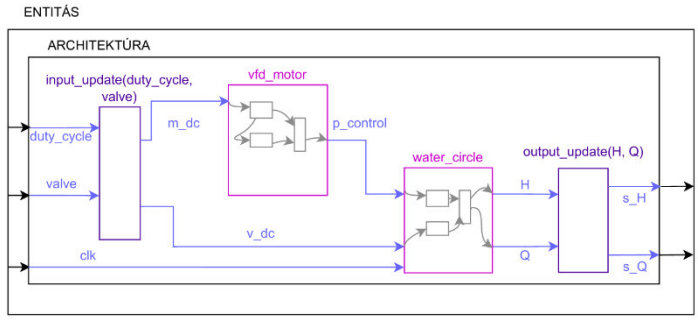

Figure 5 VHDL architecture implementing the internal structure of the HIL system [10]

As a topic of hardware implementation, the physical implementation of the system relies on three main components: the Siemens S7-1200 PLC control unit, the Digilent Nexys A7 FPGA development board, and the custom-designed level control modules. The goal was for the PLC and FPGA to communicate with each other through direct electrical signals under conditions simulating a real industrial environment. During the implementation of this, safety, galvanic isolation and distortion-free transmission of signals were the primary considerations.

4.3 Hardware Components

When choosing the tools used, preference was given to solutions that are widely used in laboratory and industrial environments. The control tasks are performed by the Siemens S7-1200 CPU 1212C PLC, which with its 24 V transistor outputs can produce PWM-based control signals and receive high-speed digital signals. The real-time running of the plant model is performed by the Digilent Nexys A7 FPGA based on the Artix-7 architecture, which provides sufficiently high computing power to run the hydraulic model and generate sensor signals.

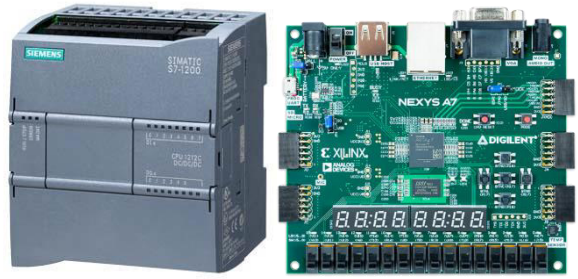

Figure 6 SIEMENS Simatic S7 1200 PLC & Digilent Nexys A7 FPGA board [1] [8]

The interface between the PLC and the FPGA is implemented by a self-designed PCB that contains optocouplers, transistor inverters and RC filters for digital and analog signal transmission. The module has a dual role: on the one hand, to coordinate voltage levels (24 V ↔ to 3.3 V), and on the other hand, to ensure galvanic isolation, which is of paramount importance for the protection of the development environment and the PLC.

4.4 Signal Transmission and Level Shifting

For the operation of the HIL environment, reliable transmission of signals between the PLC and FPGA is essential. There are three types of signals in the system: PWM-based control signals, quasi-analogue feedback signals, and simple logic status signals.

PWM based control signal (PLC → FPGA): The control of the engine speed and valve position is based on a PWM fill factor. The transistor output of the Siemens S7-1200 PLC can generate pulse signals up to 100 kHz, but a PWM frequency of 1 kHz has been used for reliable duty cycle control and level shifting. The signal is transmitted by a PC817 optocoupler, which can properly transmit PWM modulation. The signal at the output of the optocoupler is inverted, so an NPN transistor inverter restores the original logic polarity. [2]

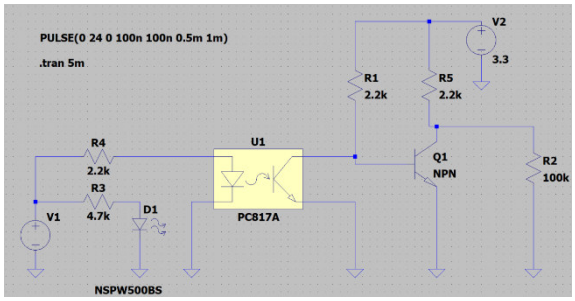

Figure 7 The optocoupler circuit [10]

Production of quasi-analog signals (FPGA → PLC): Since the FPGA cannot generate true analog signals, it generates pressure and flow values in the form of a PWM signal. The average voltage proportional to the fill factor is converted into a quasi-analog signal by a low-pass RC filter, which is amplified by an op-amp amplifier into the analog input range of the PLC from 0 to 10 V. The advantage of the solution is that the PLC treats the signal in the same way as an analogue measurement signal from a real industrial sensor.[4]

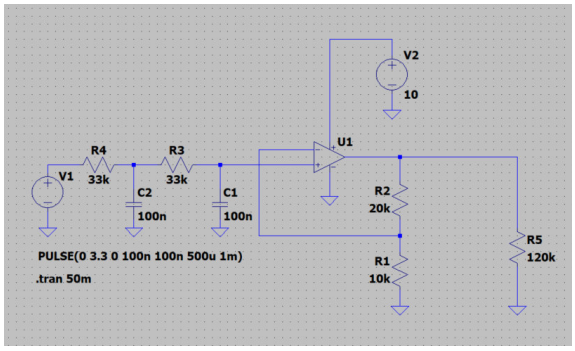

Figure 8 PWM to analog circuit [10]

Digital Status Signals (FPGA ↔ PLC): Error and status signals carry simple logical 1-bit information, so a traditional optocoupler solution can be used for matching. The 3.3V level of the FPGA is isolated by an optocoupler and matched to the 24V input level of the PLC. The inverter stage serves to restore polarity here as well.

4.5 Physical Layout

The physical design of the system is planned to carry out in a modular DIN rail arrangement in which the PLC, FPGA and level shifter modules are in separate units. This solution is easy to clarify, easily expandable and ideal for laboratory

testing. The modular design allows for future developments, such as multi-channel signal matching or the integration of additional sensor models.

5 Results

At the current stage, results are based on simulations and on hardware tests of the signal conditioning circuits. The full PLC-FPGA integration has not yet been completed, so the following findings reflect the behaviour of the verified subsystems.

.5.1 Validation of the MATLAB/Simulink Pump Model

The hydraulic model was validated by generating a Q–H curve. As the valve opening decreased, the flow rate dropped and the differential pressure increased, reproducing the characteristic behaviour of centrifugal pumps. These results confirm that the model is suitable for HIL testing, even though the FPGA implementation of the hydraulic subsystem is still under development. [11]

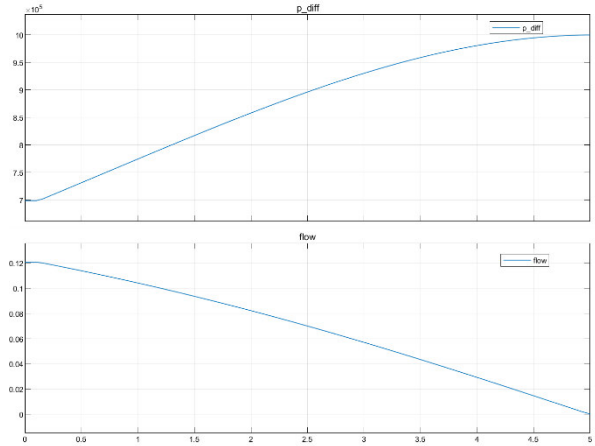

Figure 9 Differential pressure-time & Flowrate-time diagrams [10]

5.2 Testing of Signal Conditioning Modules

The interface circuits were validated in LTSpice and with physical measurements. Tests confirmed that PLC to FPGA PWM signals can be transmitted distortion-free using a PC817 optocoupler. The FPGA to PLC quasi-analog outputs can be reliably generated using PWM + RC filtering + op-amp amplification. The 1-bit

digital status signals also can be isolated and level-shifted using an optocoupler and inverter stage. These results indicate that the signal-conditioning modules form a solid basis for full system integration.

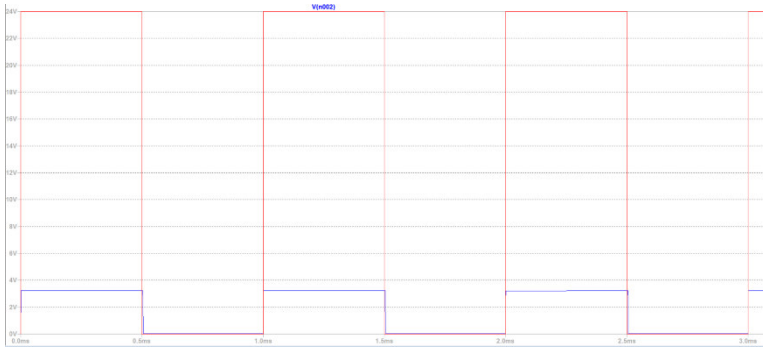

Figure 10 Input(red) & output(blue) signal of the level shifter circuit from PLC to FPGA [10]

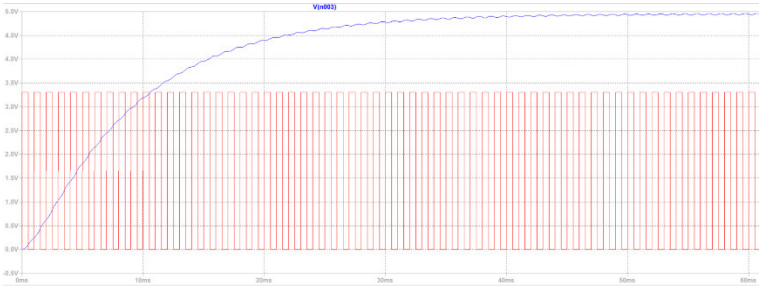

Figure 11 Input(red) & output(blue) signal of the PWM to analog circuit [10]

5.3 Status of the FPGA Implementation

The design of the VHDL-based FPGA architecture is at an advanced stage, and hardware testing has begun. According to the current state, the VHDL components of the motor and water circuit model have been completed. The internal signal management and architecture have been completed. The operation of the modules has been verified at the design level based on Simulink data, but the actual FPGA and PLC connection has not yet taken place.

In the current phase of development, simulated and partially tested results are available, and the integration and real-time verification of the entire HIL configuration will follow as a later step.

5.4 Status of the PLC Program Implementation

The first version of the PLC program to be tested has been completed, which follows a state-based structure. The PLC program is being further developed and is progressing in parallel with the preparation of the validation steps of the HIL system.

Conclusion

This work presented the development of an FPGA-based Hardware-in-the-Loop environment for the functional testing of a PLC-controlled pump performance test station. The hydraulic plant model was successfully created and validated in MATLAB/Simulink, and the required level-shifting and signal-conditioning modules were designed and tested both in simulation and hardware. Although the complete PLC–FPGA integration is still under development, the results obtained so far demonstrate that the proposed architecture can reliably reproduce the key dynamic characteristics of the test bench and can serve as a safe and flexible alternative to physical equipment during early-stage testing.

Future work will focus on completing the FPGA implementation of the hydraulic model, establishing real-time closed-loop operation with the PLC, and performing full HIL validation. The modular structure of the system enables straightforward extensions, such as the integration of multiple sensors or more detailed hydraulic components. Based on the preliminary results, the FPGA-based HIL approach shows strong potential for scalable and reproducible testing of PLC control programs in industrial environments.

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