Automatic Analog Circuit Synthesis by BF methods

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***Abstract*—As we wrote in our earlier article [10] the automatic synthesis of digital circuit is mostly solved, at a well defined boundary conditions. Algorithm of a digital topology generating can be performed. From traditional discrete electronic parts an analog circuit implementation is almost impossible,because analog integrated circuits configurable through a digital interface already exist.**

Automatic synthesis of analog circuits can be important, because are through a digital interface configurable analog integrated circuits.

All these, and increasing processing performance of computers are new approaches to be made, even the brutal force (BF) methods [23] [25].

Such synthesis may be important not only in the synthesis of discrete components, but circuit modules can be used, whether the case of configurable analog circuitry system synthesis.

In engineering practice the commonly used brute force method is very resource-intensive process.

The present article shows an optimization method by which the purely theoretical possibilities are considerably reduced thereby it increases the rate of synthesis.

In the current article, partly as a result, finished a computer program that can automatically generate circuit topologies. We will now deal with some aspects of this.

I. Introduction

An analog electronic circuit function (Γ_c) and behavior ($\mathfrak{f}$) is determined by the parameters of the used components ($\overline{\mathbf{P}}$) and the connect topology (n), according to (1);

$$\Gamma_c = \mathfrak{f}(n, \overline{\mathbf{P}}). \tag{1}$$

The circuit function is of course not an exact definition, but it can mean for example from input to output time domain determined amplitude function, frequency-domain amplitude behavior...etc. The used circuit description depends on the suspected, or the realized function of circuit [24] [26] [28].

Parameter (n) describes the network of the discrete component, in there pins are well determined connected to each other.

In equation (1) the $\overline{\mathbf{P}}$ parameter is a scalar vector, that contains the relevant parameters of used electronic parts in formal (2);

$$\overline{\mathbf{P}} \in p_0, p_1, p_2 ... p_n; \tag{2}$$

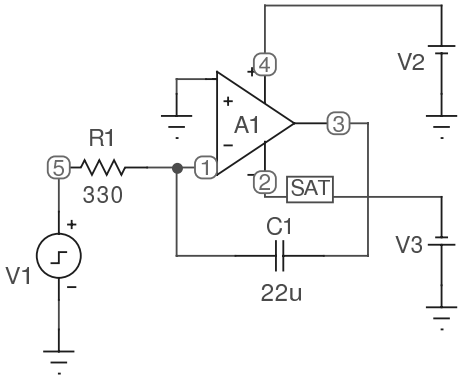

Fig. 1. Integrator circuit.

where p_n the significant parameter of electronic part, for example resistance of a resistor, capacitance of the a capacitor, h_{21} of a bipolar tranzistor...etc. [6] [22].

On Fig. 1 is seen, as above example an integrator circuit. This circuit contains an operational amplifier (A_1), a square wave input generator; (V_1) $U_{pp} = 2V$, $U_{offset} = -1V$, two power source; (V_2, V_3) with $\pm$15V, a feedback capacitor (C_1) its value is 22μF, and a resistor (R_1) and value of last one is 330Ω. These parts lists and entering a value defining of the $\overline{\mathbf{P}}$ vector [2] [3] [9].

Fig. 2 shows a connection network in short form "netlist" about of circuit of Fig. 1. This netlist describes the nods of circuits (N\$1, N\$3, N\$5). The nods N\$3 connect 2 number pads of capacitor (C_1), output of amplifier (A_1) with 4 pads of integrated circuit, and output of circuit to X_2 connector [5] [7].

Nowadays the development of such a circuit heuristic means. We know the circuit operation, the availability of parts and components to form a network with the appropriate values [16] [1]. To draw the circuit CAD tools are used, as well as circuit simulation. Network of Fig. 2 is generated from wiring diagrams[8] [4] [27] [29].

Computing environment is possible to check by circuit simulation software the operation of the realized circuit. Fig. 3 shows in time domain the circuit operation from input to output [13] [14] [15].

Net	Part	Pad	Pin
GND	IC1	1	+IN
	X1	1	S
	X2	2	S
N$1	C1	1	1
	IC1	3	-IN
	R1	2	2
N$5	R1	1	1
	X1	2	S
N$3	C1	2	2
	IC1	4	OUT
	X2	1	S
VCC-	IC1	2	V-
VCC+	IC1	5	V+

Fig. 2. A integrator circuit's connection network.

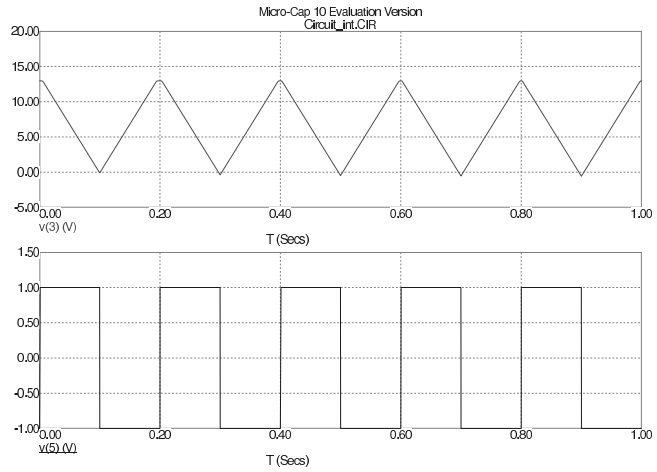

Fig. 3. Time domain simulation of integrator circuit. Bottom input signal, above the output.

II. Analog circuit realization by a switching matrix

Theoretically, if we have n numerous electronic components each of them has got ϕ_i pins which are necessary to properly connect with a wished analog circuit. If every possible way we want to create a circuit network, we need a matrix that consists of o number of columns according the (3);

$$o = \sum_{i=0}^{n-1} \sum_{j=0}^{\phi_i - 1} c_{ij}, \tag{3}$$

where for $A_{m,(i,j)}$ is true (4);

$$A_{m,(i,j)} \in [0,1]. \tag{4}$$

On Fig. 4 theoretical arrangement of a switching matrix is shown. This matrix consists of electronic parts's dev_0–dev_n leg wires as columns c_{00}–$c_{n(\phi-1)}$, and row wires for possible interconnections r_0–r_{m-1}. In (4) 0 means no connection between column and row wires, and 1 case is have got, this is actually a switch function, which is described of turned ON and OFF state. On Fig. 4 we signed this function by a switch k_g [20] [19].

It can be seen that the pins of electronic components and the interconnection wires formed from a matrix of *mxn* type, where m=n, so there is square matrix, which contains all the possible options of connections, according in equation (5):

This square matrix from equation (3) contains numerous cross points according to (6) is;

$$C_p = o^2. \tag{6}$$

Thus, the number of theoretically possible different topology (T_n) from equations (5) and (6) is;

$$T_n = 2^{C_p}. \tag{7}$$

Fig. 4 layout and description of equations (5) and (6) are so perfectionist that includes abilities of all the parts legs wires the possibility of connecting a node, as well as the possibility of all parts foot stand-alone, a unique node [18] [17].

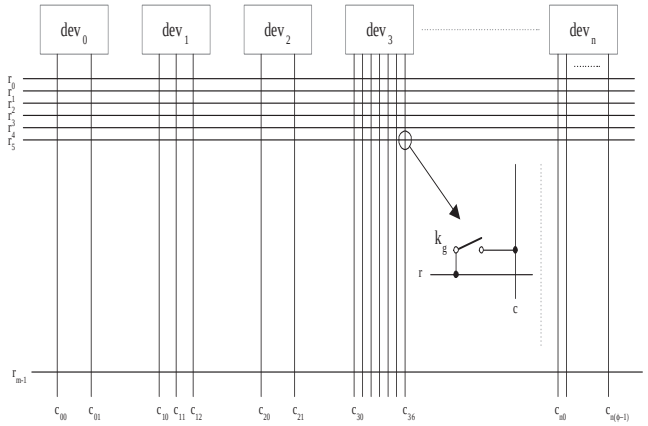

Fig. 4. Theoretical arrangement of a switching matrix for the evolving every abilities connections.

III. Optimization of a switching matrix

In the previous paragraph the possibility formation of the theoretical switch matrix is shown. According to the described solution we generate from the circuit of Fig. 1 or net list of Fig. 2 in matrix's in Fig. 5.

On Fig. 5 it can followed that every nods of netlist means a row of matrix; $r_0 = GND$, $r_1 = N\$1$, $r_2 = N\$2$, $r_0 = N\$3$, $r_0 = N\$4$, $r_0 = N\$5$. You can see that the rest of any unused nods abilities from r_6–r_{16}.

The electrotechnical or physical reason of the not used abilities is understandable, because it is meaningless to connect, for example, two power supplies (N_2, N_4), or output of operational amplifier (N_3) with input signal source (N_5). Of course one can find too much refusal of this kind.

$$A_{m,(i,j)} = \begin{bmatrix} b_{0,(0,0)} & b_{0,(0,1)} & b_{0,(1,0)} & b_{0,(1,1)} & b_{0,(1,2)} & b_{0,(2,0)} & b_{0,(2,1)}\cdots & b_{0,(n,\phi-1)} \\ b_{1,(0,0)} & b_{1,(0,1)} & b_{1,(1,0)} & b_{1,(1,1)} & b_{1,(1,2)} & b_{1,(2,0)} & b_{1,(2,1)}\cdots & b_{1,(n,\phi-1)} \\ b_{2,(0,0)} & b_{2,(0,1)} & b_{2,(1,0)} & b_{2,(1,1)} & b_{2,(1,2)} & b_{2,(2,0)} & b_{2,(2,1)}\cdots & b_{2,(n,\phi-1)} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ b_{m-1,(0,0)} & b_{m-1,(0,1)} & b_{m-1,(1,0)} & b_{m-1,(1,1)} & b_{m-1,(1,2)} & b_{m-1,(2,0)} & b_{m-1,(2,1)}\cdots & b_{m-1,(n-1,\phi-1)} \end{bmatrix}. \quad (5)$$

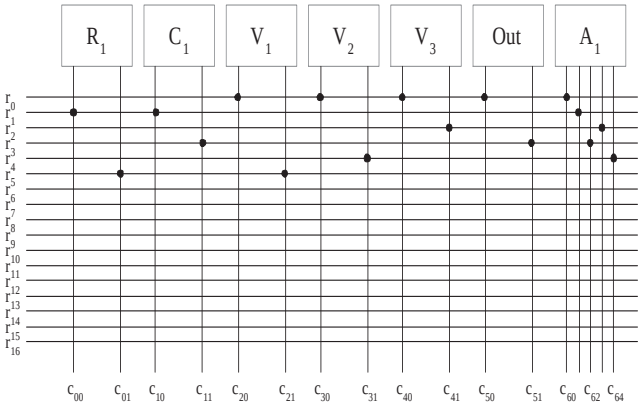

Fig. 5. Integrator circuit realization in actually connections on a switching matrix.

So our proposal is such **structural switch matrix** which can not afford such unusual theoretical, often catastrophic result inflict solution.

On the other hand, it is necessary to minimize number of cross points, because the number of ability network according to the equation (7) easy to be huge combination.

In the theoretical matrix (Fig. 5 and 5) the number of connection, according equations (6) and (7) was: $r_{m-1} \cdot c_{n(\phi-1)}$, actually in examples are $C_p = 17^2, C_p = 289$ so the abilities topology are $T_n = 2^{289}, T_n = 9,94 \cdot 10^{86}$.

These values at the proposed structural switch matrix are in order to form; $C_p = 17 \cdot 10, C_p = 170$, and $T_n = 2^{170}, T_n = 1,49 \cdot 10^{51}$. The different according T_n parameter in 10^{35}.

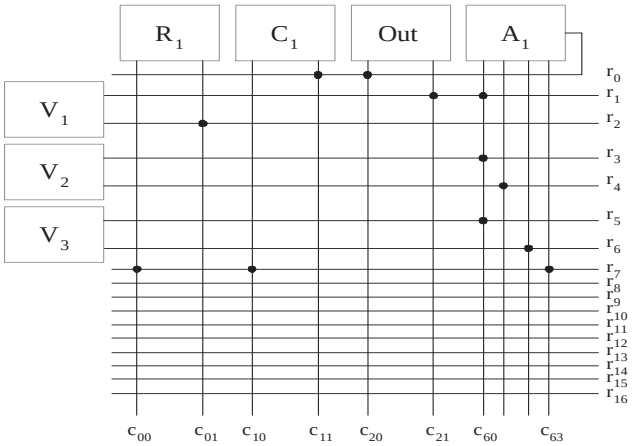

Fig. 6. Integrator circuit realization on structural switching matrix.

Other mitigation options appropriate management of common GND node, and self-evident is providing of active device's power supply [11] [12].

A special heuristic approach is the elimination of not used rows of matrix, on Fig 6 from $r_8 - r_{16}$. So the number of T_c is "only" $1,2 \cdot 10^{24}$.

IV. Automatic Synthesis by Brutal Force methods

Based on the principles described in the previous chapter created a computer program using the structural switch matrix-oriented aspects. The main screen of running netlist generator-program shown on Fig 7, and on Fig 8 are seen a part of generated netlist directories [21].

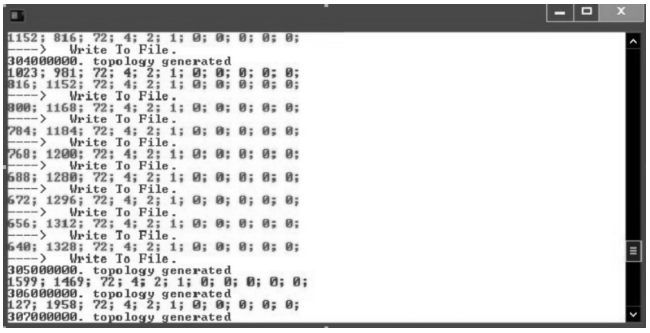

Fig. 7. Main screen of topology generator program.

The generated files are all made the right format, so called CKT, for Spice (MICROCAP-10) circuit simulation program. This standard format shows Fig 9.

Together with the generated files clearly describe the circuit topology, the circuit graphic display can also be important. Is a free program can help solve the visualization of the connection of circuit, with using some circuit macros. On Fig 10 sows any random topology of generated netlist files.

Of course, each of Fig 9 has a netlist format a real elements feasible circuit, but they are usually unnecessary to show. However, the practicing engineer with more information is

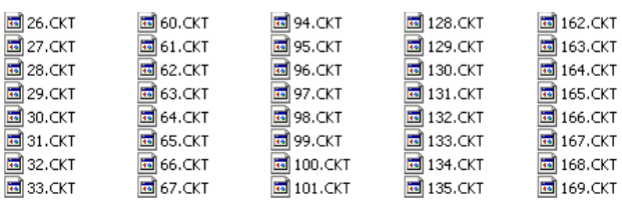

Fig. 8. A part of generated netlist file's directory.

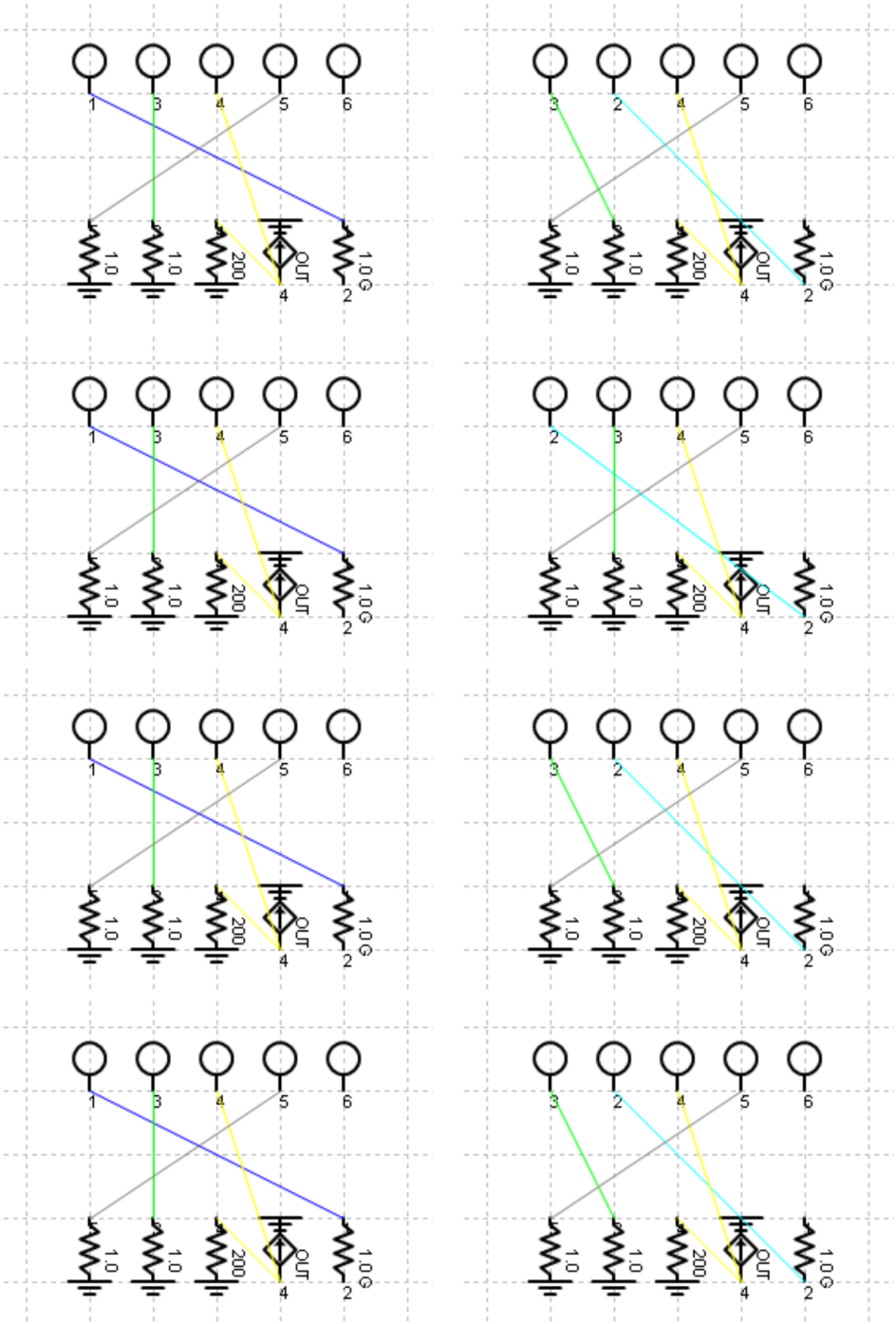

Fig. 10. Any automatically generated ”integrator” circuits on a Netlist-viewer program’s screen. On upper side of figures there are from 1–6 poles of ability nodes of integrator of Fig. 1.

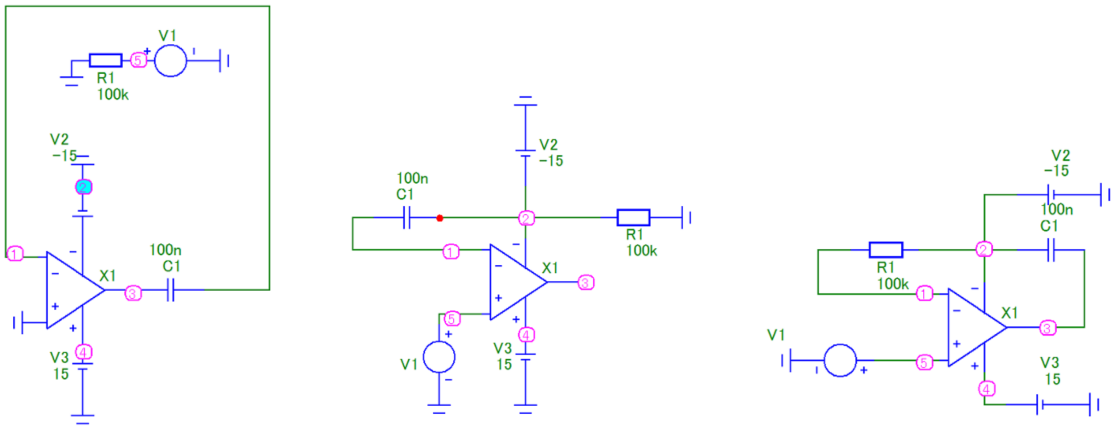

Fig. 11. Three wrong ”integrator” circuit in Micro-Cap simulation environment.

displayed in the traditional circuit diagrams, some examples of which are shown in Fig 11.

V. Conclusions

The previously proposed structured switch-matrix we can generate a combinatorial topology wit an appropriate computer program. Later we can analyze with a circuit simulation method the function of generated circuit, and the appropriate parametric fine settings carried out. This article provides a solution the applicability of high performance computers and advanced cross-bar switch circuits appearance. The proposed methods are extendable for the system generated from functional blocks, and subsystems too.

Further work is needed to search for efficient algorithms, and exclusion of generating the self understood wrong circuits.

```
;$10100001000
;$00001010000
;$00000000010
;$00010100100
;$00000000001
;$01000000000
;$00000000000
;$00000000000
;$00000000000
;$00000000000
;$00000000000
*
*
*
X1 1 0 3 2 4 LM741
U3 4 0 DC 15
U2 2 0 DC -15
C1 0 3 100N
R1 0 5 100K
U1 5 0 DC 0 PULSE 0 1 0.05 0.032001 1 29.918 32
*
*
*
.SUBCKT LM741 2 1 4 3 5
RSUPPLUS 5 0 1
RSUPMIN  3 0 1
ROUT 4 0 200
GOUT 0 4 1 2 1000
RIN 1 2 1G
.ENDS LM741
*
*
.END
;$SpiceType=SPICE2G
```

Fig. 9. A standard file format (CKT) for Spice-like circuit simulations program..

References

[1] N. Ádám. Single input operators of the df kpi system. *Acta Polytechnica Hungarica*, 7(1):73–86, 2010.

[2] A.S. Deese, C.O. Nwankpa, J. Jimenez, J. Berardino, and J. Hill. Design of modular field programmable analog array hardware for analysis of large power systems. pages 1207–1210, 2012.

[3] Gy. Györök, M. Makó. Configuration of EEG input-unit by electric circuit evolution. *Proc. 9th International Conference on Intelligent Engineering Systems (INES2005)*, pages 1–7, September 2005.

[4] Gy. Györök, M. Makó, J. Lakner. Combinatorics at electronic circuit realization in FPAA. *Acta Polytechnica Hungarica, Journal of Applied Sciences*, 6(1):151–160, 2009.

[5] Gy. Györök. The function-controlled input for the IN CIRCUIT equipment. *Proc. 8th Intelligent, Engineering Systems Conference (INES2004)*, pages 443–446, September 2006.

[6] Gy. Györök. Self configuration analog circuit by FPAA. *Proc. 4th Slovakien – Hungarien Joint Symposium on Applied Machine Intelligence (SAMI2006)*, pages 34–37, January 2006.

[7] Gy. Györök. Self organizing analogue circuit by monte carlo method. *Proc. IEEE International Symposium on Logistics and Industrial Informatics (LINDI2007)*, pages 34–37, September 2007.

[8] Gy. Györök. A-class amplifier with FPAA as a predictive supply voltage control. *Proc. 9th International Symposium of Hungarian Researchers on Computational Intelligence and Informatics (CINTI2008)*, pages 361–368, November 2008.

[9] Gy. Györök. The FPAA realization of analog robust electronic circuit. *Proc. IEEE Internacional Conference on Computational Cybernetics (ICCC2009)*, pages 1–5, November 2009.

[10] Gy. Györök. Crossbar network for automatic analog circuit synthesis. *Proceedings (Liberios Vokorokos, Ladislav Hluch, Jnos Fodor szerk.) of the IEEE 12th International Symposium on Applied Machine Intelligence and Informatics (SAMI 2014). IEEE Computational Intelligence Society, Budapest: IEEE Hungary Section, ISBN:978-1-4799-3441-6*, pages 263–267, January 2014.

[11] J. Kopják. Dynamic analysis of distributed control network based on event driven software gates. *IEEE 11th International Symposium on Intelligent Systems and Informatics, Subotica, Serbia*, ISBN: 978-1-4673-4751-8:p. 293–297, 2013.

[12] J. Kopják and J. Kovács. Implementation of event driven software gates for combinational logic networks. *IEEE 10th Jubilee International Symposium on Intelligent Systems and Informatics, Subotica, Serbia*, ISBN: 978-1-4673-4751-8:p. 299–304, 2012.

[13] K. Lamár. A világ leggyorsabb mikrovezérlöje. *ChipCAD Kft.*, page 96, January 1999.

[14] K. Lamár and Veszprémi K. A mikroszámítógépek térnyerése a villamos hajtások szabályozásában. *Proceedings of the Kandó Conference 2002, Budapest, Hungary*, pages 1–7, January 2002.

[15] L. Madarász and Zivcak J. Aspects of computational intelligence: Theory and applications. *Revised and Selected Papers of the 15th IEEE International Conference on Intelligent Engineering Systems 2011, Springer-Verlag , Berlin Heidelberg*, ISBN 978-3-642-30667-9:p. 436, 2011.

[16] L. Madarász and Fözö R. Intelligent technologies in modelling and control of turbojet engines. *New Trends in Technologies : Control, Management, Computational Intellingence and Network Systems, Rijeka, Croatia*, ISBN 978-953-307-213-5:p. 17–38, 2011.

[17] David L. Alderson Paul J. Nicholas. Fast, effective transmitter placement in wireless mesh networks. *Military Operations Research*, 17.(4.):pp. 69–84, 2012.

[18] Malcolm Bailey David A. Foster Peter R. Green, Peter N. Green. Design and delivery of a microcontroller engineering teaching theme. *International Journal of Electrical Engineering Education*, 50.(3.):pp. 231–238, 2013.

[19] A. Pilat and J. Klocek. Programmable analog hard real-time controller [programowalny sterownik analogowy]. *Przeglad Elektrotechniczny*, 89(3 A):38–46, 2013. cited By (since 1996) 0.

[20] Adam Pilat. Control toolbox for industrial programmable analog controllerembedding state feedback controller. pages 1–4, 2012.

[21] P. Rideg. Combinatorial analog circuit synthesis. *Obuda University, Alba Regia University center, Bs.C Thesiswork-2014, suprvisor: Gy. Györök.*

[22] S. Sergyán. Edge detection techniques of thermal images. *2012 IEEE 10th Jubilee International Symposium on Intelligent Systems and Informatics, SISY 2012*, pages 227–231, 2012.

[23] S. Sergyán. Useful and effective feature descriptors in content-based image retrieval of thermal images. *LINDI 2012 - 4th IEEE International Symposium on Logistics and Industrial Informatics, Proceedings*, pages 55–58, 2012.

[24] J. Tick. User interface redesign based on user behavior analyses. *Proc. of ICCC 2003 IEEE International Conference on Computational Cybernetics (ICCC2003)*, pages 29–31, October 2003.

[25] J. Tick. *Potential Application of P-Graph-Based Workflow in Logistics*. Aspects of Computational Intelligence: Theory and Applications: Revised and Selected Papers of the 15th IEEE International Conference on Intelligent Engineering Systems 2011, pp. 293-303, Springer Verlag, 2012, Heidelberg; London; New York, 2012.

[26] J. Tick. Business process-based initial modeling at software development. *Proc. of IEEE 11th International Symposium on Applied Machine Intelligence and Informatics (SAMI2013)*, pages 141–144, January 2013.

[27] Z. Vámossy. Thermal image fusion. *2012 IEEE 10th Jubilee International Symposium on Intelligent Systems and Informatics, SISY 2012*, pages 385–388, 2012.

[28] L. Vokorokos, N. Ádám, and B. Madol. The process control for p-single operators. *19th International Workshop on Robotics in Alpe-Adria-Danube Region, RAAD 2010 - Proceedings*, pages 119–123, 2010.

[29] Y. Wang, M. Zhu, J. Cui, H. Lin, and Y. Jiang. Current-mode reconfigurable analog circuit for analog signal processing. *Nanjing Hangkong Hangtian Daxue Xuebao/Journal of Nanjing University of Aeronautics and Astronautics*, 43(4):532–537, 2011.