Charging behaviour of MNOS memory devices with embedded Si nanocrystals: Experiments and computer simulation

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***Abstract*— Memory window width of MNOS memory devices depends on the geometrical parameters of the applied structure and the electric field in the oxide layer. The charging behaviour of these memory devices can be improved by applying Si nanocrystal layer. Here the results of experiments and the computer simulation performed for the understanding the obtained behaviour, are presented.**

I. INTRODUCTION

Information storage in non-volatile memories is based on changing the threshold voltage of field effect transistors (FETs) by appropriate voltage pulses. The actual mechanism is injection of charge by tunneling and its storage in a floating gate (see "Fig. 1,") or in traps located in the insulator layer in MNOS (see "Fig. 2,") or SONOS (see "Fig. 3,") structures. The reduction of the dimensions of floating gate memory FETs is limited mainly due to reliabity problems connected with defects in the tunneling layer, because the reduction of lateral dimensions calls forth the reduction of oxide thickness. So, if there is a defect or week point in the thin oxide layer, the whole charge can be lost via it. Replacement of the floating gate with isolated semiconductor nanocrystals (NCs) is a possible and successful way for solution of this problem [1,2]. The loss of information via defects in oxide layer can also be avoided by using MNOS or SONOS structures, because traps, where the charge is stored, are separated a priori.

Formation of semiconductor nanocrystals can improve the behaviour of these structures as well. So, Si nanocrystals were embedded in MNOS structures at the oxide/nitride interface, and - as expected - improved memory behaviour were obtained for structures with certain geometrical parameters [3]. As a next step of optimization, an additional thin nitride layer was grown between the oxide layer and the sheet of embedded Si nanocrystals. Here the results of experiments and the computer simulation performed for the understanding the obtained behaviour, are presented.

II. EXPERIMENT AND SIMULATION DETAILS

Two different layer structures have been pared grown on n-type Si substrates: 1) SiO_2 (2.5 nm)/Si NC/Si_3N_4 (40 nm) structures consist of a thin SiO_2, a Si nanocrystal and a Si_3N_4 layers. 2) SiO_2 (2.5 nm)/Si_3N_4 (3 nm)/Si NC/Si_3N_4

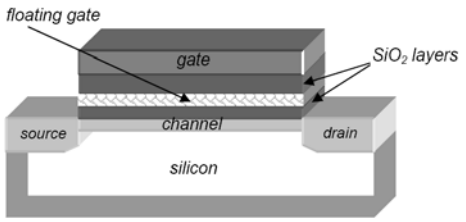

Figure 1. The floating gate field effect transistor

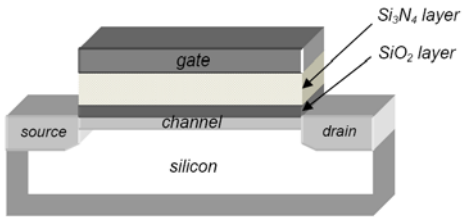

Figure 2. The MNOS memory transistor

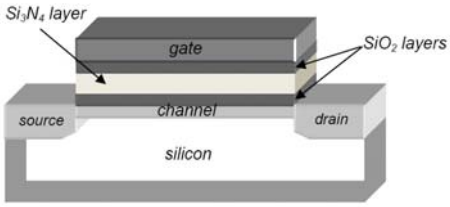

Figure 3. The SONOS transistor

(35 nm) structures consist of a thin SiO_2 and a Si nanocrystal layer embedded between two Si_3N_4 layers. Reference samples without nanocrystals were also prepared.

The Si nanocrystal layers have been prepared by LPCVD from SiH_2Cl_2. [3,4] The Si_3N_4 layers have been prepared by LPCVD from NH_3 and SiH_2Cl_2. The SiO_2 layers have been prepared by chemical treatment using HNO_3 [3-5].

The effect of the duration of nanocrystal deposition has been investigated. Memory window behaviour were studied experimentally, as a function of writing/aresing voltage pulse amplitude with charging pulse width of

10 ms. (Memory window is the change of flat-band voltage of MNOS capacitors after application of consequtive writing/aresing voltage pulses with the same amplitude.)

The tunneling probability of electrons to the conduction band of the nitride layer has been calculated. On the basis of WKB approximation [6], the tunneling probability of electron through a potential barrier with arbitrary shape can be expressed as

$$T = \frac{e^{-2\int_{x_1}^{x_2} dx \sqrt{\frac{2m}{\hbar^2}(V(x)-E)}}}{\left(1+\frac{1}{4}e^{-2\int_{x_1}^{x_2} dx \sqrt{\frac{2m}{\hbar^2}(V(x)-E)}}\right)^2}$$

where T is the tunneling probability, x_1 and x_2 are the coordinates where the electron enters and leaves the potential barrier (see "Fig. 4,"), m is the effective mass of the electron, $\hbar$ is the Planck constant (devided by 2π), $V(x)$ is the potential energy as a function of coordinate, and E is the electron energy.

The band diagram of the MNOS structure used in the calculations is presented in "Fig. 4." The tunneling probability of electrons has been studied as a function of the oxide thickness and of the location and size of nanocrystals.

III. Results

The memory window obtained for the SiO_2/Si NC/Si_3N_4 structures with Si NC deposition duration of 0 s, 30 s and 60 s are shown in "Fig. 5,". Longer duration deposition resulted in increasing NC density, which yielded wider memory window.

The memory window of the SiO_2/Si_3N_4/Si NC/Si_3N_4 structures with nanocrystal size of 5 nm and 8 nm are presented in "Fig. 6,". The memory window for structures with Si NCs is about two times wider than that for the reference sample without nanocrystals.

The calculated probability of electron tunneling to the conduction band of the nitride layer in MNOS structures without nanocrystals as a function of the oxide thickness and the electric field in the oxide layer is presented in

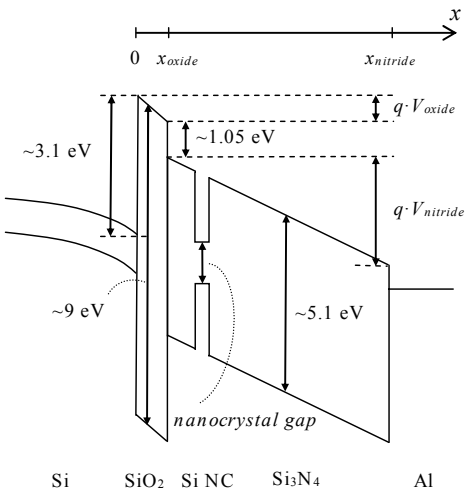

Figure 4. Band diagram of MNOS structures with Si nanocrystals used for the calculation of electron tunneling probability.

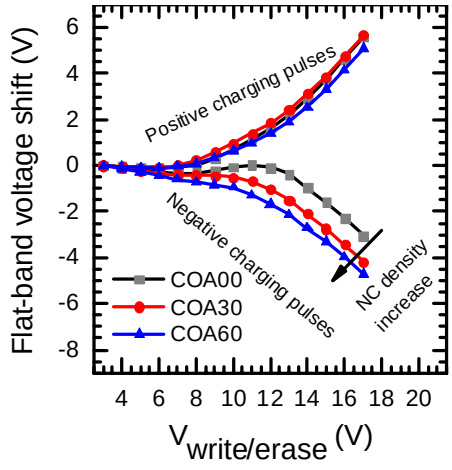

Figure 5. Memory window of the SiO_2/Si NC/Si_3N_4 structures with Si NC deposition duration of 0 s, 30 s and 60 s (COA00, COA30 and COA60, respectively). Charging pulse width is 10 ms.

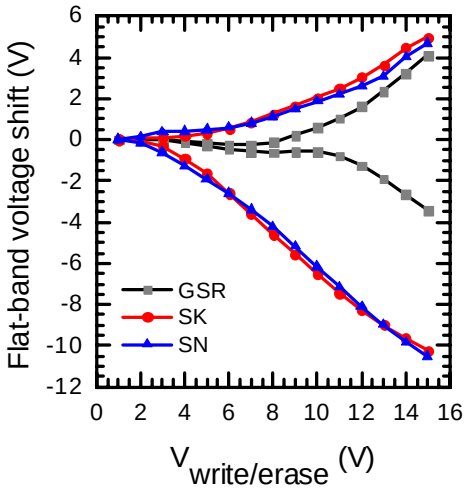

Figure 6. Memory window of the SiO_2/Si_3N_4/Si NC/Si_3N_4 structures with different nanocrystal size: SK 5 nm, SN 8 nm, GSR - reference sample without nanocrystals.

"Fig. 7,". The tunneling probability exhibit maximum as a funciton of oxide thickness. This maximum is closer to the Si/SiO_2 interface for higher electric fields. The increase of tunneling probability in the presence of a thin oxide layer in comparison with MNS structures without oxide layer, is due to a high potential drop on the oxide layer caused by its lower dielectric constant.

"Fig. 8," presents the calculated probability of electron tunneling to the conduction band of the nitride layer in MNOS structures with Si nanocrystals as a function of the nanocrystal layer thickness and the electric field in the oxide layer, for nanocrystal layer located at the SiO_2/Si_3N_4 interface or at a distance of 3 nm from the interface in the nitride layer. The oxide thickness used in the calculation is 2.5 nm.

Comparing tunneling probabilities presented in "Figs. 7 and 8", it can be seen that the presence of Si nanocrystals in the vicinity of the SiO_2/Si_3N_4 interface strongly enhances the tunneling probability of electrons to the nitride conduction band. If nanocrystals are more far from the Si surface, the tunneling probability is lower.

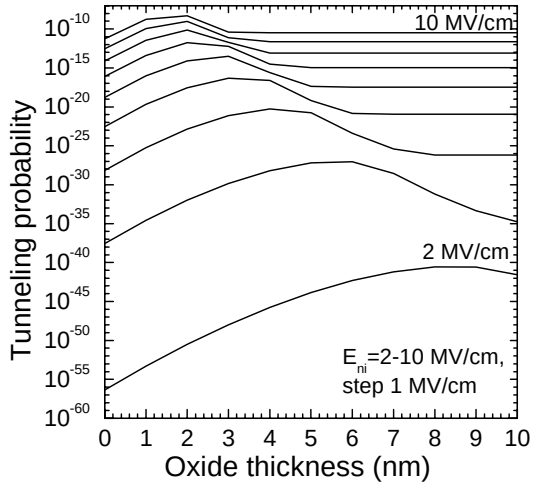

Figure 7. Electron tunneling probability to the conduction band of the nitride layer in MNOS structures without nanocrystals as a function of the oxide thickness and the electric field in the oxide layer.

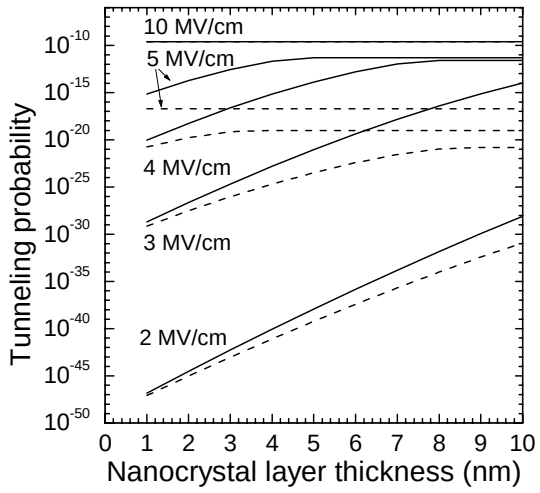

Figure 8. Electron tunneling probability to the conduction band of the nitride layer in MNOS structures with Si nanocrystals as a function of the nanocrystal layer thickness and the electric field in the oxide layer for nanocrystal layer located at the SiO_2/Si_3N_4 interface (solid lines) or at a distance of 3 nm from the interface in the nitride layer (dashed lines). The oxide thickness used in the calculation is 2.5 nm.

IV. CONCLUSIONS

A properly located layer of Si nanocrystals can improve the charging behaviour of the MNOS structures.

Memory window width of about 15 V has been achieved for charging pulses of ±15 V, 10 ms.

The optimal charging behaviour of MNOS structures can be expected for oxide thickness of 2-3 nm.

The presence of Si nanocrystals in the vicinity of the SiO_2/Si_3N_4 interface strongly enhances the tunneling probability of electrons to the nitride conduction band.

The improved charging behaviour of $SiO_2/Si_3N_4/Si$ NC/Si_3N_4 structures in comparison with SiO_2/Si NC/Si_3N_4 structures cannot be explained by the increased tunneling probability of electrons.

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